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Byeong-Mun Song, Robert McDowell,
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GENERAL ATOMICS
Energy Products
SORRENTO ELECTRONICS
4949 GREENCRAIG LN, SAN DIEGO, CA 92123-1506
858.522.8400
www.ga-esi.com

Practical Design and Control of a ZVS 3-Level DC-DC Converter With Minimum Circulating Current

Byeong-Mun Song, Robert McDowell, Andy Bushnell, and Joel Ennis

General Atomic Energy Products
Sorrento Electronics, Inc.
4949 Greencraig Lane, San Diego, CA 92123 USA
byeong-mun.song@sorrento.com, www.gaep.com

Abstract: **This paper describes a practical design and control of a newly developed zero-voltage-switching (ZVS) 3-level dc-dc converter with minimum circulating current. The converter is designed with ZVS soft-switching techniques to achieve high efficiency. Furthermore, two main key issues on the high voltage dc-dc converter are discussed with minimization of the circulation current between main switches and optimal dead time for soft switching. The converter has achieved about 95% efficiency under wide 7kW load condition.**

Index Terms: **3-Level dc-dc converter, ZVS converter, dc power supply, soft-switching converter.**

I. Introduction

Isolated high voltage step-down dc-dc converters are not popular in industry due to requiring a high conversion ratio between high input and low output voltage. Because most of these converter topologies have potential high transient voltage on main switches caused by the existence of the transformer leakage inductance.

To overcome the problem associated with high transient voltage stress, soft-switching 3-level converter topologies are alternative choice for medium power dc-dc power conversions [1]-[2]. These converters mostly employ a phase-shift control method to achieve ZVS conditions to the primary switches. However, such a phase-shift control method inevitably provides a circulating current path through the transformer and primary power stage during freewheeling period, resulting in increase of conducting losses in the converter [3]. In order to block or minimize the circulating current, various auxiliary circuits with active switch and/or passive components are added to the secondary side on the converter [4]-[6]. It can be achieved better efficiency of the converter.

However, when the switching frequency of the converter increases up to nearly 100kHz, such manners are not only the penalty of inefficiency of the additional auxiliary circuit due to loss of duty cycle but also the penalty of the cost on the converter [7].

In this paper, a zero-voltage-switching 3-level dc-dc converter with minimum circulating current is proposed for 7kW power supplies. The work mainly focuses on practical design criteria for minimizing circulating current of the converter without any additional components. The converter is verified with optimization of a dead time for soft-switching under load variations and with minimization of leakage inductance of a transformer.

Furthermore, practical design, analysis, and implementation of the converter will be fully characterized including the design of transformer and controller. The overall performance of the converter will be presented.

II. ZVS 3-Level DC-DC Conveter

A. Main Circuit

Figure 1 shows a ZVS 3-level half-bridge converter for soft switching. The converter consists of two power stages, high and low voltage. The high voltage stage is with four main switches, two blocking diodes and a flying capacitor to ensure the voltage sharing across the blocking switches. It is possible to allow the operation of the converter with a phase-shifting control, so that the converter can achieve soft switching for the inner switches of S_2 and S_3 by using the leakage inductance in the transformer. The low voltage stage is connected to the center-tapped windings of the transformer along with an output filter composed of L_o and C_o. In the main circuit, the dc split capacitors C_1 and C_2 establish a voltage midpoint between 0 and the input dc voltage. The switch pairs, S_1 and S_4, and S_2 and S_3, are alternately turned on and off for a given interval.

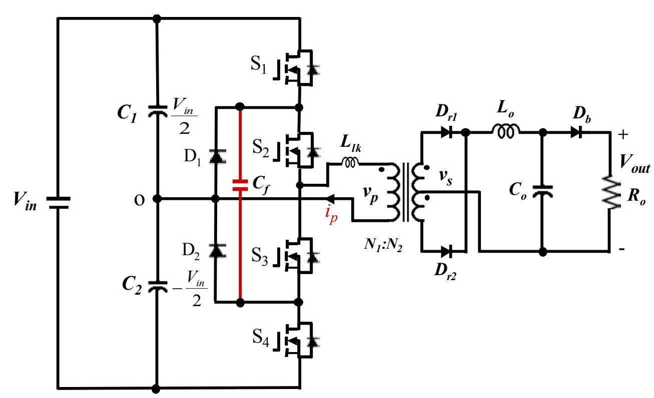


Figure 1. ZVS 3-level dc-dc converter for soft switching.

With bi-directional current paths, the flying capacitor should be charged or discharged depends on the voltage conditions to make the voltage balancing between the switching cells. The balanced voltage serves as the blocking voltage of S_2 and S_3 at turnoff, and provides a solution for the unbalancing problem between the dc split capacitors. In addition, D_b internally blocks against reverse power flow.

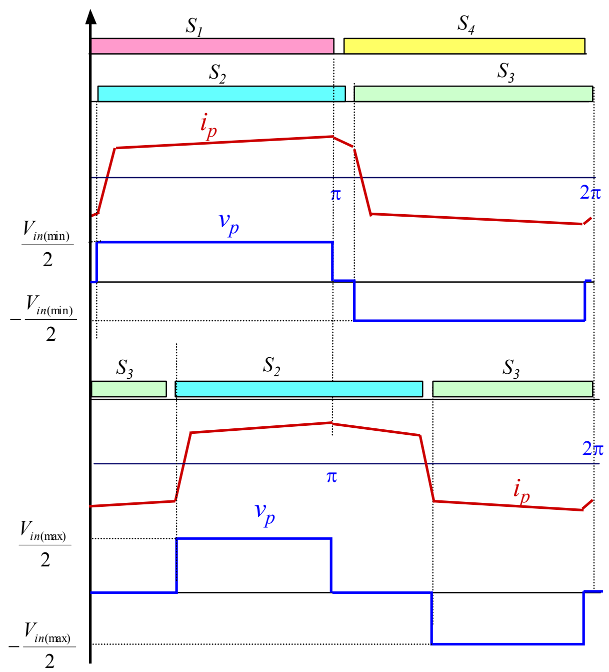


Figure 2. Corresponding voltage and current waveforms of the converter.

B. Operational Principle

Figure 2 shows the switching sequences of the converter, which has four different operational modes to achieve the desired output voltage waveforms at stead state operations.

1) Mode I: When S_1 and S_3 are conducting, the diode of D_1 is blocking the current path and the output voltage becomes zero. If the flying capacitor voltage, v_{Cf}, is lower than the voltage across the dc split capacitor of C_1, the flying capacitor is charged through $C_1 \rightarrow S_1 \rightarrow C_f \rightarrow D_2$.

2) Mode II: When S_1 and S_2 are conducting, the current directly flows to the transformer and the output voltage of the transformer becomes $V_S/2$.

3) Mode III: In this mode, S_2 and S_4 are conducting. The current path is blocked by the diode of D_2 and the output voltage becomes zero. Like Mode I, if the flying capacitor voltage, v_{Cf}, is lower than the voltage across the dc split capacitor of C_2, the flying capacitor is charged through $C_2 \rightarrow D_1 \rightarrow C_f \rightarrow S_4$.

4) Mode IV: When the top switch S_1 and S_2 are turned off and the bottom switch S_3 and S_4 are turned on, the voltage charged in C_2 is used to provide power to the transformer. At this mode, since the voltage across the transformer feeds to the negative rail, the current path is negative and the output voltage becomes $-V_S/2$.

III. Practical Design Procedures

The design procedures begin with the converter specifications. Considering the input and output voltage characteristics, the key design criteria are described.

A. Design Specifications

In the design, when the input voltage range is considered to be from about 850V to 1250V, the actual voltage range for operation of the converter should be greater than the required maximum voltage and should be lower than the minimum voltage. At the rated output power, the converter is maintained a certain output voltage of 68V with the given ripple and voltage regulation specifications. Selecting the output filter, which consists of output inductor and capacitor highly depends on ripple and regulation. As a baseline, 2% ripple and 5% voltage regulation specifications are considered. The design life of the converter is also considered for a naval ship design life of 30 years along with the efficiency greater than 95% from half to full load.

On the other hand, the converter is internally required with protection against reverse power flow and will be hot swappable. In addition, the converter provides uninterrupted power to mission-critical loads to allow the system to overcome the any fault situations for the system.

Furthermore, all these alternatives have compromises in size, weight and efficiency constraints, and the functionalities of the converter should be addressed along with controller design.

B. Transformer Design

The design of a transformer is critical to the success of the converter performance. The transformer requires high voltage conversion ratio to nominal 900V to 68V, but worse in reality. The following discussions give a step-by-step procedure for the design of a 7kW transformer operating at 80 kHz.

Step 1: Determine an effective duty cycle of the 3-level half-bridge converter, D_{eff}:

$$D_{eff} = \frac{2 \cdot N_t \cdot V_{out(rms)}}{V_{in(\min)}} = \frac{2 \cdot N_t \cdot 68}{735} = 0.185 \cdot N_t \qquad (1)$$

where, N_t is the turn ratio of transformer, (N_1/N_2), and $V_{in(\min)}$ is the minimum dc bus voltage, 735V. In order to minimize a circulating current through the transformer, it is required to a highly maximum duty value of D_{eff}. If $N_t = 5$, the effective duty cycles under different conditions are:

$$\begin{aligned} D_{eff(\max)} &= \frac{2 \cdot N_t \cdot V_{out(rms)}}{V_{in(\min)}} = \frac{2 \cdot 5 \cdot 68}{735} = 0.925 \\ D_{eff(\min)} &= \frac{2 \cdot N_t \cdot V_{out(rms)}}{V_{in(\max)}} = \frac{2 \cdot 5 \cdot 68}{1{,}250} = 0.544 \end{aligned} \qquad (2)$$

Step 2: Calculate a required core effective area, A_e:

$$A_e = \frac{V_{in(\max)} \cdot (D_{eff(\min)}/2)}{N_1 \cdot B_m \cdot f_s} \times 10^8$$
$$= \frac{1{,}250 \times 0.272 \times 10^8}{N_1 \times 2{,}000 \times 80{,}000} = \frac{213}{N_1}(cm^2) \qquad (3)$$

If $N_1 = 20$ and $N_2 = 4$, the required core effective area is obtained as A_e = 10.7 cm^2. The chosen core parameters are following as:

- Selected A_e : 15.7 cm^2
- Core dimension : 4" × 2.319" × 4"
- Model no. : E 100/28

Step 3: Determine the current ratings of the primary and secondary windings, respectively:

$$i_{out} = \frac{P_o}{V_{out} \cdot \eta} = \frac{7{,}000}{68 \times 0.95} = 108A$$
$$i_p = D_{eff(\max)} \cdot \frac{I_{out}}{2 \cdot N_t} = 0.925 \cdot \frac{108}{2 \cdot 5} = 10A \qquad (4)$$

Step 4: Select winding gages

The Litz wire cables are selected due to high frequency transferring. With 80kHz operation, the AWG 38 (d = 0.1mm, 0.031 A @ 500 cir. mil/A) is chosen in both the primary and secondary windings; primary winding of 700 turns and secondary winding of 3,600 turns.

On the other hand, it is required that a small leakage inductance can reduce the effective duty cycle loss, which increases the conduction loss caused by the circulating current. But, when the inductance is so small, it is may be difficulty to realize ZVS for the main switches at light load condition.

C. Minimum Circulating Current

It is well known that the phase-shifting converter can be operated with circulating currents though the transformer. During regulation, the phase shift reflects as a circulating current, so that the level of circulating current is restricted by provision of the transformer. In order to minimize the circulating current on the converter, it is necessary to maximize the turn ratio of transformer as mentioned in the previous section, and to optimize this dead time for the soft-switching converter. In this section, the dead time, t_d, should be designed with the converter circuit as follows:

$$t_{d(\min)} > \frac{L_{lk} \cdot I_p}{V_{in(\min)}/2 - 2 \cdot V_{drop}} = 270 \text{ ns} \qquad (5)$$

where, V_{drop} is the device drop voltage for each conducting device, about 1.5V at the load current of 10A, L_{lk} is the leakage inductance, 10μH, including the transformer and its wiring, and I_P is the primary current of the transformer, 10A.

If the dead time, t_d, is long enough, the soft-switching circuit in which consisting of L_{lk} (= 10μH) and the internal capacitance of the MOSFET, C_{mos} (= 18nF), resonates at its resonant frequency. However, if t_d is small, C_{mos} is not completely discharged under light load condition. Thus, the dead time for soft-switching operations is limited to a minimum load current. So, its time should be considered within 500ns in this design.

D. Main Switch and Diode Selection

For the 7kW 3-level converter, use of MOSFET seems a better choice because of high switching capability over 100kHz. The MOSFET has a low voltage drop to a high voltage dc bus and has low switching losses during high switching operations. To select the voltage rating of the MOSFET, an 800V device is selected based on the 3-level converter topology for a maximum input voltage of 1,250V. In this design, the 800V - 40A MOSFET device module (APT8015JVFR) with SOT-227 package case is selected. For the low side blocking diode, SOT-227 Schottky diode module (150V-2*110A, APT2×100D20J) with SOT-227 package case is selected for reducing the conducting voltage. A fast rectifier module (400V - 200A, HFA 200MD 40C) with a fast reverse recovery time is selected for the secondary rectification.

E. Clamping Circuit

The clamping circuit consists of two blocking diodes and a flying capacitor. The flying capacitor across the blocking diodes can provide the phase shifting current path to the inner loop switches during freewheeling modes, so that the soft-switching operation can be achieved to the converter. This tends to improve the efficiency of the converter. For voltage blocking, an ultra fast recovery diodes module with 30A – 1000V (APT30D 100BHB) is selected.

On the other hand, to select the capacitance of the flying capacitor, it is important to the capacitor to be stable at any operation condition. It guarantees the voltage stability of the converter. With voltage stability, the capacitor voltage is subjected to the variation of the load current, even when the average of the current is zero. The capacitance is related to current and voltage ripple of the capacitor. Thus, the capacitance can be calculated as:

$$C_f \geq \frac{i_p \cdot t_d}{\Delta V_{Cf}} = \frac{10 \times 500 \times 10^{-9}}{2} = 2.5 \ \mu\text{F} \qquad (6)$$

In the design, an 800V - 3μF capacitor is chosen to the converter.

F. Controller Design

It is evident that the performance of soft-switching converters highly depends on the controller design. The controller provides gate drive signals to the converter. To accomplish the successful operation, voltage and current feedbacks and protection signals are incorporated to secure the operation of the converter, feeding to the controller.

Figure 3 shows a control block diagram for the converter. The control diagram is designed with a proportional-integral (PI) controller to regulate the output voltage. The output voltage is controlled by the control command, which is generated by comparing the voltage reference with the actual output voltage signal, $V_{out(act\_cmd)}$.

In the design, the amplitude of the voltage reference is limited to 1V, which R_{r1} and R_{r2} form a voltage divider from internal 5V supply in the UCC3895. The actual output voltage signal is set to 1V to 68V output during nominal operation. If the output voltage goes beyond 71V, or below 65V, then its fault signal is activated. This tends to stabilize the output voltage at any conditions for the converter. At the brown out condition, which a slow reduction in input voltage causes a problem of fault, the controller is also incorporated with the logic necessary to resolve this condition.

For the voltage control, V_{out} is sensed from a voltage divider of R_u and R_b and fed to the error amplifier though the isolated amplifier, and its output sent to the comparator, which compares the programming voltage of V_{ref} with $V_{out(act\_cmd)}$. The error voltage in the error amplifier is fed to the PWM comparator for a phase shifting between the switches. The parameters of the PI controller are selected along with the 80kHz switching. The controller zero and pole frequencies, f_z and f_p, are calculated as:

$$f_z = \frac{1}{2\pi \cdot R_2 \cdot C_1} = 318 \quad Hz$$
$$f_p = \frac{1}{2\pi \cdot R_2 \cdot C_2} = 32 \quad kHz \qquad (7)$$

where, R_1 = 1 kΩ, R_2 = 50 kΩ, C_1 = 0.01μF, and C_2 = 100 pF. In this design, the cutoff frequency of f_c = 10kHz is selected for the 80kHz converter.

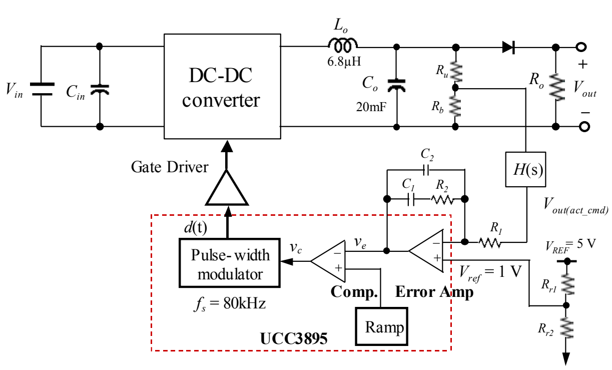
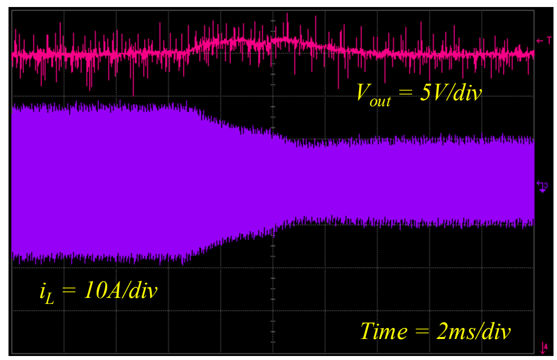


Figure 3. Control block diagram for the converter.

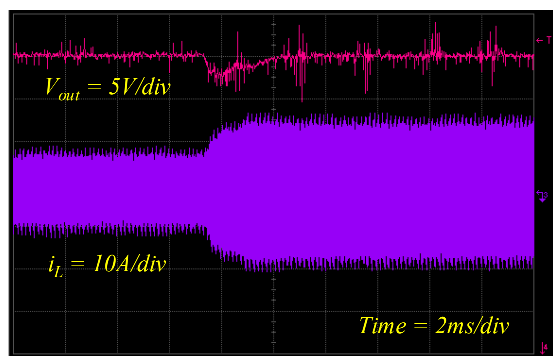
IV. Experimental Results

In order to validate the converter operation, various experiments were conducted. The parameters are selected as V_{in} = 800V, C_1 = C_2 = 130μF, C_f = 3μF, C_O = 20mF and L_O = 6.5μH.

Figure 4 shows the output voltage waveforms of the converter under load transients. When the load changes from 100% to 50%, the output voltage shown in Figure 4(a) is followed to the controller, and the voltage variation was within 1.8V peak during 5ms, 2.6% of V_{out}. Figure 4(b) shows that the output voltage also follows up to the load step change when the load changes from 50% to 100%. The step response time is 3ms and the voltage overshoot is within 2.5V, 3.6% of V_{out}. These results are satisfied to the specification of 5% regulation while the load is stepped from 50% to 100% to 50%. The transient response magnitude can be reduced if additional capacitors are installed at the output of the converter. But the settling time will be increased.



(a) Load change from 100% to 50%



(b) Load change from 50% to 100%

Figure 4. Load transient characteristics of the converter.

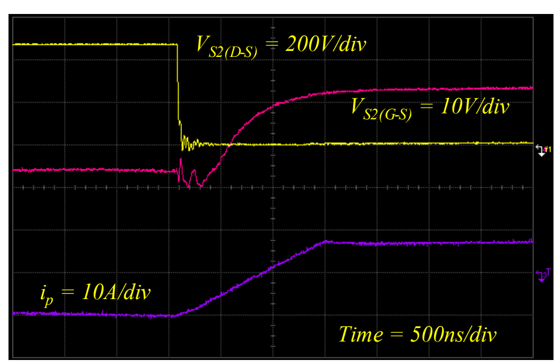


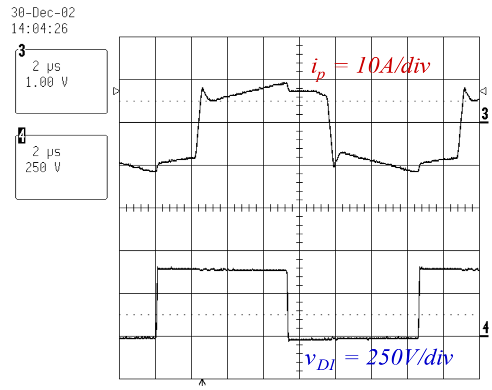
Figure 5. Zero voltage switching waveforms of S_2 during turn-on.

Figure 6. Photograph showing the converter.

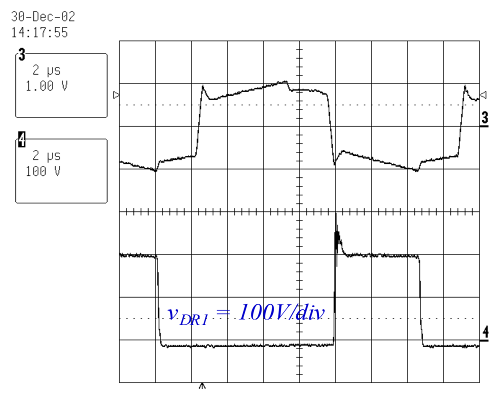
Figure 5 shows the experimental waveforms of the drain-to-source voltage, $V_{S2(D\text{-}S)}$, gate-to-source voltage, $V_{S2(G\text{-}S)}$ and primary current, I_p. During turn-on, when $V_{S2(D\text{-}S)}$ reaches zero, $V_{S2(G\text{-}S)}$ is turned on at the zero voltage condition. Thus, the ZVS was achieved with the experiment. It can eliminate the turn-on switching loss during switching. Figure 6 shows a photograph of the converter. The converter is designed for 7kW ship electric power distribution systems.

Figure 7 shows the experimental key waveforms of the converter. Each waveform indicates its corresponding part of the converter at the same primary current. For the blocking diode operation as shown in Figure 7(a), when the regulation starts to regulate the output voltage the blocking diode of D_1 is conducting and D_2 is blocking. The blocking voltage is clamped with the 400V for the 800V input. Figure 7(b) and (c) show the voltage waveforms of the secondary rectifying diode, V_{Dr1} and V_{Dr2}. The diode of D_{r1} is conducting for a period when the switch pair, S_1 and S_2, are turned on, and D_{r2} for S_3 and S_4. During the primary voltage of the transformer is zero, the circulating current continuously flows through the primary winding. It is the penalty associated with a circulating current, so that the level of circulating current is restricted. On the other hand, the voltage spikes in both D_{r1} and D_{r2} are observed under the experiment test. These spikes due to the leakage inductance of the transformer and the parasitic capacitance of the rectifying diode on the secondary side were reduced by a RC snubber circuit. With an additional soft-switching circuit, it can eliminate the spike. Figure 7(d) shows the voltage waveform of the flying capacitor across the blocking diodes. The voltage ripple is within 5V under the selected 3μF capacitor. Adding more capacitance of the flying capacitor can reduce its voltage ripple. Figure 7(e) shows the output voltage waveforms of the converter. The waveform confirms the operation of the dc-dc converter to be constant 68V output. The small output voltage ripple is achieved within ± 1% at the rated output voltage.

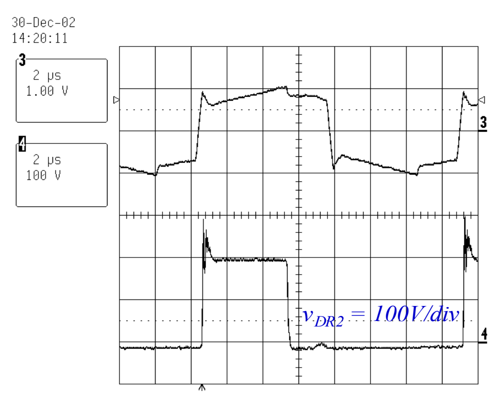
Figure 8 shows the primary voltage waveforms of the transformer under different dead time. Since the dead time between the main switches in the converter is reflected to the soft-switching operation, it is necessary to optimize the time. As expected, when t_d = 500ns is chosen, there is glitch on the voltage waveform as shown in Figure 8(a). On the other hand, when t_d = 430ns is chosen, the waveform as shown in Figure 8(b) is clean without any voltage dip. Thus, the dead time is optimized with the values of L_{lk} and C_{mos}. Figure 8(c) summarize the experimental measured efficiency of the converter under different dead time. With t_d = 430ns, the efficiency of the converter is 95.5% at full load condition, and 95.7% at 50% condition. These efficiencies are included all power converter module components, as a photograph shown in Figure 4. However, at light load region, a large dead time like t_d = 500ns can be achieved a better efficiency to the converter.



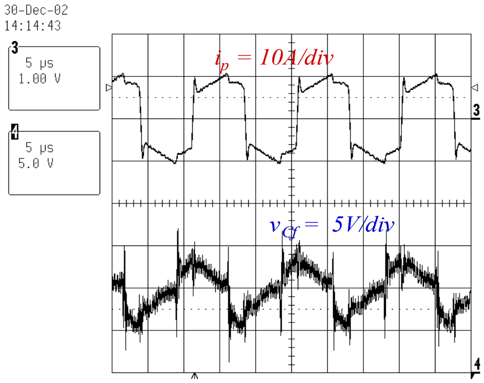
(a) Voltage waveform of V_{D1}



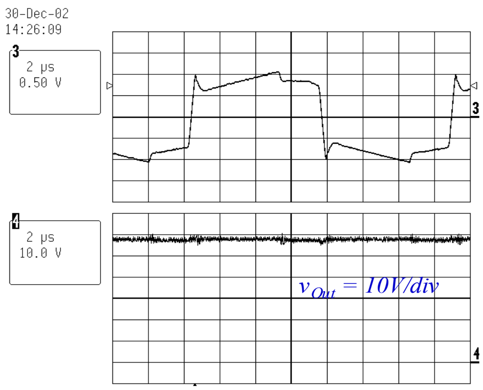
(b) Voltage waveform of V_{Dr1}



(c) Voltage waveform of V_{Dr2}

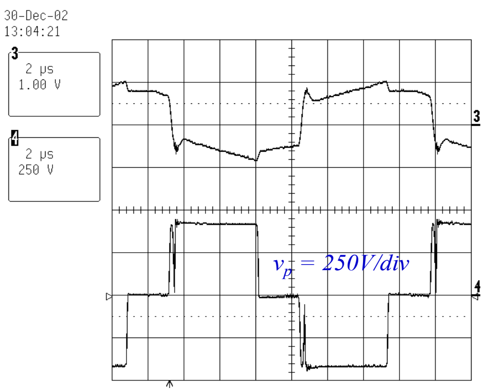


(d) Flying capacitor voltage waveform

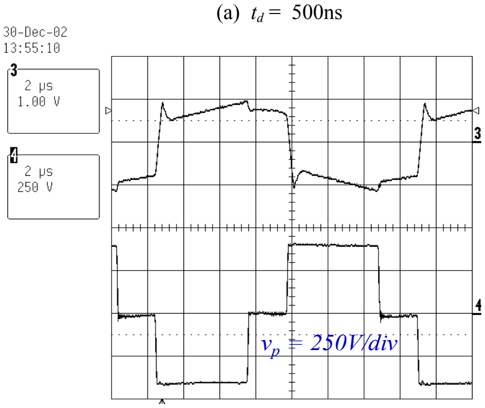


(e) Output voltage waveform

Figure 9. Key waveforms of the converter.



(a) t_d = 500ns



(b) t_d = 430ns

Figure 10. Primary current and voltage waveforms of the transformer under different dead time

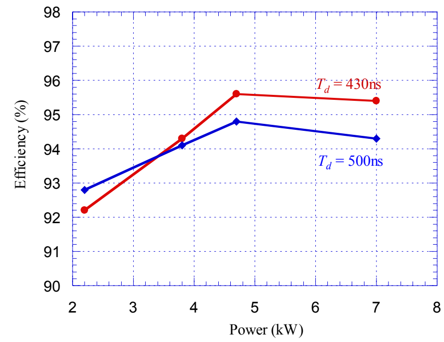


Figure 11. Efficiencies of the converter under different dead time.

V. Conclusion

A newly developed ZVS 3-level dc-dc converter with minimum circulating current has been fully characterized with practical design and control for high voltage power supplies. The various practical design criteria including transformer, main components, clamping circuit, and controller have been discussed with experimental results. Furthermore, to minimize the circulating current through the primary transformer and main switches, the design of the transformer and dead time for soft switching were optimized with the resonant circuit. Thus, the converter has achieved over 95% efficiency by the significant reduction of the switching losses without any additional auxiliary circuit.

With the merits of simplicity and high efficiency, the proposed converter shows excellent performance and potential for various industry applications.

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